CLAIMS

1.   A method of reading data in a virtual ground array of memory cells comprising:

sensing substantially simultaneously a state of adjacent memory cells, wherein a bit stored in each cell of said adjacent memory cells is in an identical state.

2.   The method of claim 1, wherein said sensing substantially simultaneously comprises:

coupling a sense amplifier to a first source/drain terminal of each cell of said adjacent memory cells;

setting a voltage at a second drain/source terminal of each cell of said adjacent cells to a read level; and

sensing in a reading direction the state of said adjacent cells.

3. The method according to claim 1, wherein said adjacent cells share at least a word line.

4. The method according to claim 1, wherein said adjacent cells share at least an inside bit line.

5. The method according to claim 1, wherein said coupling a sense amplifier to a first source/drain further comprising coupling said sense amplifier to a shared bit line of said adjacent cells.

6. The method according to claim 1, wherein said coupling a sense amplifier to a first source/drain further comprising coupling said sense amplifier to bit lines of said adjacent cells that are not shared by said adjacent cells.

7. The method according to claim 1, wherein any one of said memory cells stores at least one bit in said charge trapping region.

8. The method according to claim 1, wherein said adjacent cells are sensed with substantially identical current.

9. The method according to claim 1, wherein said memory cells are nitride read only memory (NROM) cells.

10. The method according to claim 1, wherein said coupling a sense amplifier to a first source/drain further comprising coupling said sense amplifier through select transistors to said shared or not shared bit lines.

11. The method according to claim 1, wherein said coupling a sense amplifier to a first source/drain further comprising coupling said sense amplifier substantially directly to said not shared bit lines.

12. A method of programming at least a pair of adjacent memory cells, the method using programming pulses applied to either a drain or a gate of at least a pair of adjacent memory cells.

13. The method according to claim 12, wherein said programming pulses are applied simultaneously to said adjacent memory cells.

14. The method according to claim 12, wherein said programming pulses are serially applied to said adjacent memory cells.

15. The method according to claim 12, wherein said programming pulses are serially applied to groups of said adjacent memory cells, wherein for each group said programming pulses are simultaneously applied.

16. The method according to claim 12, wherein said programming pulses are directed in said reading direction.

17. The method according to claim 12, wherein said programming pulses are directed in a direction opposite to said reading direction.